Amendments to the Specification

Please amend the specification as follows:

Replace the paragraph starting at page 6, line 23

Referring to FIG. 3, a slice of the switching core 20 includes an STS input mode control circuit 29 and write address generator 26 that controls a flow for writing the data on input bus 21 into the data memory block 23. Memory block 23 includes one or more RAMs (not shown). The STS input mode control circuit 29 is capable of storing a binary bit of information for every STS input of the switch. Switching core 20 also includes a connection random access memory (RAM) 28 capable of storing a binary bit (provisioning bit 30) of information for every STS output of a VT switch device. Provisioning bit 30 specifies which outputs are sourced as STS connections. The switching core also includes a data memory block 23 that includes one or more RAMs for switching data. Connection RAM 28 controls reading of data out of memory block 23. The slice of the switching core 20 also includes other blocks to manage the switching of data. For example, the switching core 20 includes a swap control module 22, a read ~~access~~ address generator 24, and a read address translator 27. The read address translator 27 can be used to map or translate the read addresses emerging from the read address generator 24. Translation may be required if the memory within the data memory block 23 is allocated based on signal type as per the provisioning stored in the STS input mode control block 29.

Replace the paragraph starting at page 9, line 14

In both these examples, the provisioning bit 30 is set to indicate a VT source and the provisioning bit is not set to indicate an STS-only source where the state of the bits could be changed. If the state of the bits is changed, the provisioning bit 30 is set to indicate an STS-only source and the provisioning bit is not set to indicate a VT source.

Replace the paragraph starting at page 9, line 28

FIG. 4 shows an example mapping 50 including a VT input 52 to the switch, a VT output 62 of the switch, an STS input 64 to the switch, and an STS output 70 from the switch. As described in one example above, in order for the switch to assemble synchronized outputs that include STS-only and VT sources with associated latencies, the input frames including VT

sources have their pointer adjusted at the VT switch input. Based on the state of provisioning bit 30, the switch determines if the output is being sourced from an STS input or a VT input. An example of a VT-mapped input to the switch 52 shows the VT-mapped inputs have their SPE (i.e. 28 bytes of VT data 56) fixed to an advanced pointer. For example, the VT frame inputs have their payload which starts with J1 byte rolled back 58 from position 60a (pointer offset '522') to position 54a (pointer offset '492'). After switching, the J1 byte at location 54a is in location 54b in output 62. Likewise, VT data 56b in output 62 is delayed compared to VT data 56a in input stream 52. If the input is an STS entry, the data is read out of the data memory one timeslot after it is written. For example, the overhead 66a (labeled A1, A2, and J0) and the SPE area 68a in STS mapped input 64 are each shifted by a single timeslot (i.e. one STS-1 byte number) to locations 66b and 68b in the STS mapped output 70. The adjustment of the pointer for the VT sources results in no apparent frame skew between the VT mapped output 62 and the STS mapped output 70 (as shown by line 72).